Electronic Version
Stylesheet Version v1.1.1

CHIP-PACKAGING WITH BONDING OPTIONS HAVING A PLURALITY OF PACKAGE SUBSTRATES

Abstract

Chip-packaging with bonding options having a plurality of package substrates. The chip-packaging includes first and second package substrates, a chip, and a lead frame. The chip having a plurality of bonding pads is mounted on the first package substrate. One of these bonding pads is connected to the first package substrate. Another bonding pad is connected to the second package substrate. The lead frame is connected to one bonding pad. The first and second package substrates have first and second voltages, respectfully. The first voltage and the second voltage are different, and each can be a GND voltage or a POWER voltage. With connection of these bonding pads with the lead frame or connection of these bonding pads with two package substrates, input ends or output ends in the chip could be connected to a GND voltage or a POWER voltage, or to one pin of the chip-packaging.